a 1.2v 10-bit 165msps video ADC

This paper depicts A 10-bit 165MSPS ADC design is presented in this paper. It is an ultra-low-power, low area design that operates with single 1.2V supply voltage for Digital and Analog.

Hyma B R
Shibin P V
Ramya Nair S R
Roni Vincent
Rajagopal P C
QuEST Global

contents

A 1.2V 10-bit 165MSPS Video ADC

Abstract

A 10-bit 165MSPS ADC design is presented in this paper. It is an ultra-low-power, low area design that operates with single 1.2V supply voltage for Digital and Analog. This ADC is single-ended and uses time-interleaved SAR architecture. It also provides calibration for offset correction.

***Keywords* — Time-interleaved, Video ADC, SAR.**

I. INTRODUCTION

The demand for high-speed signal processing applications such as high definition Analog front-ends requires ADCs which meet the characteristics of low power consumption, high resolution and high speed of operation. The ADC presented in this paper is a 10-bit SAR based ADC that allows to have very low power consumption and sampling rate as high as 165MSPS. It occupies low area and operates with single supply voltage for Digital and Analog. It also offers rail-to-rail input range and doesn't need any coupling capacitor at the input.

The ADC is designed using Fujitsu 65nm CMOS (CS200L) technology with MIM capacitors. It finds application in LCD flat panel monitors, Video projectors, Plasma display panels, Video capture hardware etc. Table 1 shows the brief specification of the ADC.

Parameter	ADC Specification			Unit
	Min	Typ	Max	
Supply Voltage	1.14	1.2	1.26	V
Temperature range	-40		125	℃
Supply Current		6	13	mA
Resolution		10		bits
INL	-2		2	LSB
DNL	-1.5		1.5	LSB
SINAD @ 10MHz	53			dB
Layout Area	360000			μm^2
Process	Fujitsu 65nm			

Table 1 Specification of the proposed ADC.

II. TIME-INTERLEAVED ARCHITECTURE

Typically the high sampling rate ADCs are built using either Flash or Pipe-line architecture. But they are usually power hungry designs. In this paper we are presenting an alternate solution to address the long haunting problem faced by the industry. Here instead of Pipe-line or flash architecture we opted to use SAR time interleaved architecture which scales down with technology and is advantageous in terms of area and power consumption.

Time-Interleaving is a smart technique to achieve an overall high sample rate by operating low sample rate ADCs in parallel. In a time-interleaved architecture, a system of n parallel ADCs are used which alternately take one sample (time-interleaved sampling) at a time. Fig. 1 gives the block diagram of the proposed time-interleaved ADC. It uses n number of 10-bit SAR ADCs in time interleaved fashion. Thus each ADC samples data every n-th cycle of the effective sample clock. The result is that the sample rate is increased n times compared to what each individual ADCs can manage.

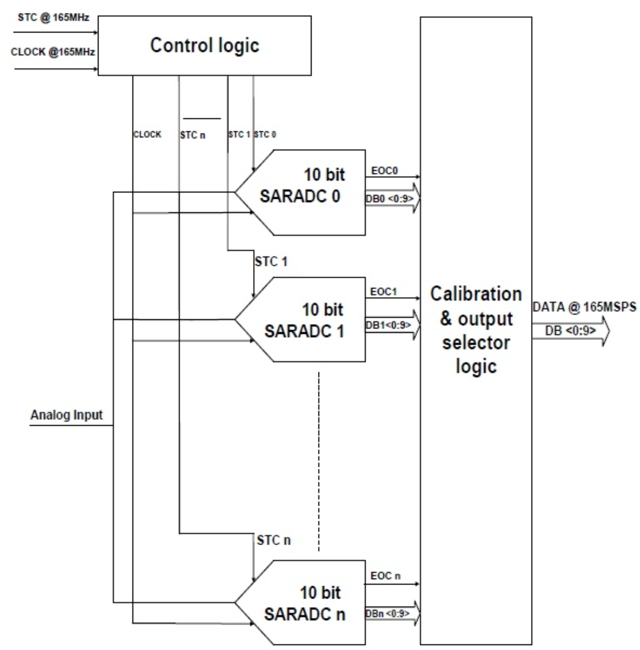

Fig 1 Block diagram time-interleaved ADC.

A 1.2V 10-bit 165MSPS Video ADC

III. SINGLE 10-BIT SAR ADC OPERATION

For the unit ADC design, SAR architecture is preferred over other co-existing ADC architecture since it is illustrious for minimum power consumption design. The architecture selection is based on having more "digital" sections rather than "analog" sections. SAR ADC meets this requirement, as the comparator is the sole "analog" component in this design, the rest of the modules shrink as the design is implemented in contemporary technologies (low). Due to the digital nature, reduced power supply can be used resulting in further power reduction. The sampling speed required is very high and SAR ADC cannot meet that specification but using the Time-Interleaved approach several low power SAR-ADCs can be placed in parallel to achieve High Sampling rate. Table 2 shows the comparison of various ADC architectures.

Fig 2 shows the block diagram of a 10-bit SAR ADC. A successive-approximation ADC basically consists of a comparator, Digital to Analog Converter (DAC) and a Successive Approximation Register (SAR). It uses the comparator to successively narrow a range that contains the input voltage. At each successive step, the converter compares the input voltage to the output of the internal DAC which might represent the midpoint of a selected voltage range. At each step in this process, the approximation is stored in the SAR. The steps are continued until the desired resolution is reached. Thus for a 10-bit SAR ADC digital data is available after 10 clock cycles. Thus an SAR ADC basically implements a binary search algorithm.

Architecture	Speed	Conversion Time	Resolution	Area	Power
Flash ADC	High	Constant	Low (up till 8-bits)	Increases exponentially with resolution	Very high
Pipelined ADC	medium-high	Increases with resolution	medium-high (up till 12-bits)	Increases linearly with resolution	medium
Sigma-Delta ADC	medium	Trade-off with resolution	High (up till 24-bits)	constant;no change with increase in resolution	medium-low
SAR ADC	medium-low	Increases with resolution	High (up till 18-bits)	Increases linearly with resolution	medium-low

Table 2 Comparison of various ADC architectures.

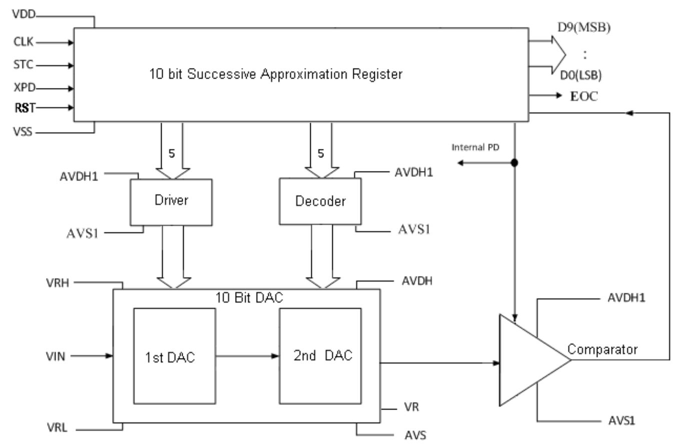

Fig 2 Single ADC Block diagram

To achieve best compromise on performance and size, a combination of resistor strings and weighted capacitors are used to digitize the input voltage level. In a 10-bit resolution of the ADC, the 10 bit SAR forms the core logic of unit ADC, it decides the configuration of DAC based on the comparison result from the comparator. The macro operates at 1.2v supply. The RDAC and CDAC together forms the DAC section of unit ADC.The driver is used to drive the switches within CDAC.The decoder decodes the code for the RDAC coming from the digital section and drives the RDAC section accordingly. The higher 5 bits are converted by the capacitor network and the lower 5 bits by resistor string. Special techniques are adopted to enhance the performance of the unit ADC and there by increase the speed for the unit SAR ADC.

In the proposed design we employ n ADCs in a time interleaved fashion, in such a way that, effectively we can obtain ADC output in each clock cycle.

A 1.2V 10-bit 165MSPS Video ADC

IV. CONTROL LOGIC

The external STC (Start Conversion) signal will be divided into n internal STC's using control digital logic to trigger unit ADC operation. This block is made dependent to RST (Reset) and XPD (power down) signals, so that during power down or reset operation whole n ADC'c will be disabled

V. OUTPUT SELECTION LOGIC

Individual Data outs [0:9] of unit ADCs will be available on each clock cycle. Correct data corresponding to each ADC will be routed to output using Output selection logic. Here the EOC (End of Conversion) signal generation also takes place.

VI. CALIBRATION OPERATION

As the ADC is basically targeting video application, bottom level signal variants are of at most importance. In order to incorporate a perfect signal conversion operation at low voltage levels (which represent black variants in a video signal) the ADC is equipped with a custom offset correction mechanism.

The fully custom calibration technique can compensate for negative as well as positive offset errors. This smart technique keeps this ADC in a competent position in the analog video front end arena. Another important feature of this custom compensation technique is its ability to compensate for ADC mismatches due to temperature variation in real operating conditions.

Calibration operation is based on a robust algorithm which takes care of all the conditions which may lead to errors in ADC operation due to offset or temperature variation. Temperature variation effects are monitored by a reference ADC which is positioned in a manner to accommodate the temperature change effects of all the operating ADCs.

The calibration process operates in the background to normal ADC operation and monitor for periodic variations on ADC offset due to temperature, process and supply fluctuations. Periodic calibration is done based on the calibration cycle which is defined internally by the calibration system.

The calibration operation happen at every calibration cycle and the ADC output gets updated with the trailing signal of calibration cycle.

Error accumulated due to temperature variation is calibrated periodically at calibration cycle. In analog correction, the correction factor is used to select the required offset voltage to the respective ADCs. In digital correction, the calibrated ADC output is derived by applying the correction factor to the actual ADC output.

Calibration operation can be bypassed by applying an active high external asynchronous signal on CALBYP (Calibration Bypass) pin. Valid data is made available at the ADC output at the rising edge of EOC.

VII. SIMULATION RESULT

Two ADC macros have been incorporated in the TEG chip - 165MSPS ADC & 130MSPS ADC as shown in Fig 6 .The switching between two ADC's are decided by the Mode control pin which is further controlled by power down signals of two ADC's. ADC's characteristics such as INL/DNL (Fig 5), SINAD, ENOB (Fig 3 and Fig 4) simulation result is listed in Table.1.

A 1.2V 10-bit 165MSPS Video ADC

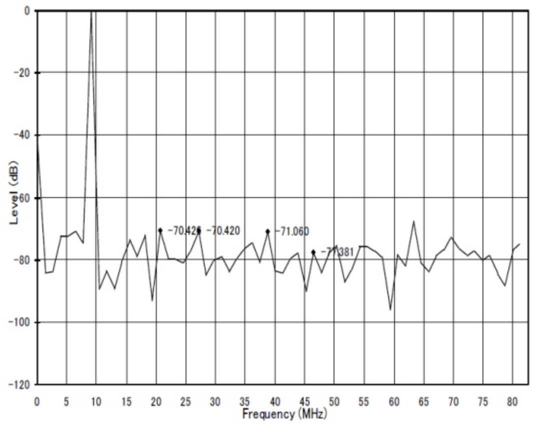

Fig 3 FFT Result with Fin =10MHz.

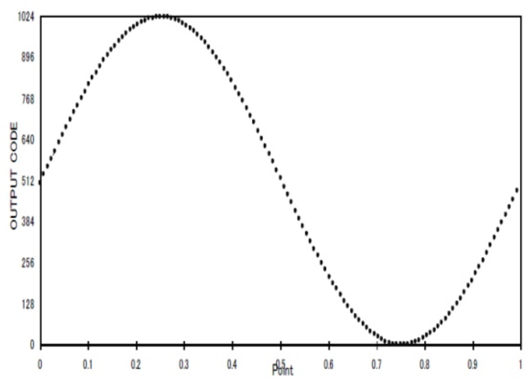

Fig 4 Output Waveform result With Fin = 10MHz

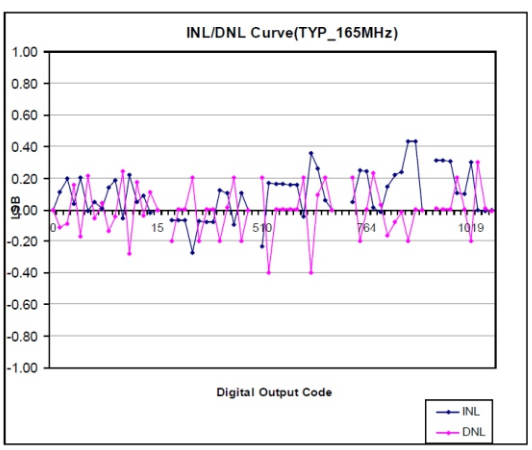

Fig 5 INL/DNL Graph @ Typical 1.2V 165MSPS

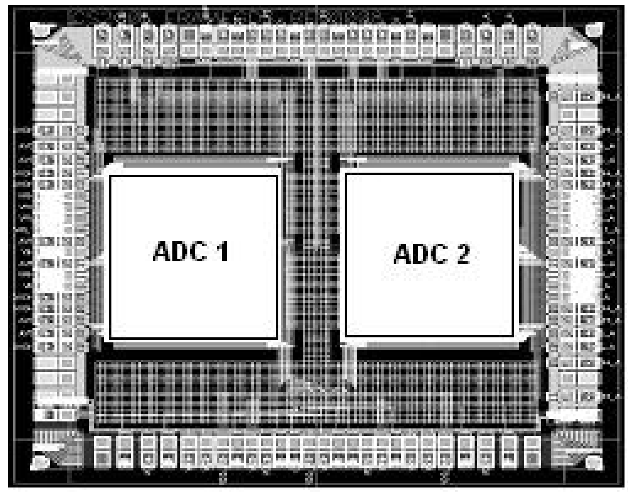

Fig 6 TEG chip Layout

Special care was taken while doing the macro layout. The CLK tree, STC routing was provided symmetrically to all n ADCs to avoid unwanted switching and delay issues between ADC which inturn can affect overall system performance.

VIII. CONCLUSIONS

In this paper a 10-bit 165MSPS time-interleaved SAR ADC with low power consumption is presented. The custom calibration technique enables the successful compensation of the offset and temperature variation errors. Time-Interleaving enabled the SAR ADC to have high sample rate.

The high frequency operation and offset compensation techniques make this ADC suitable for video front end application in high definition display. Fig 7 shows the Evaluation board set up of VADC macro.

A 1.2V 10-bit 165MSPS Video ADC

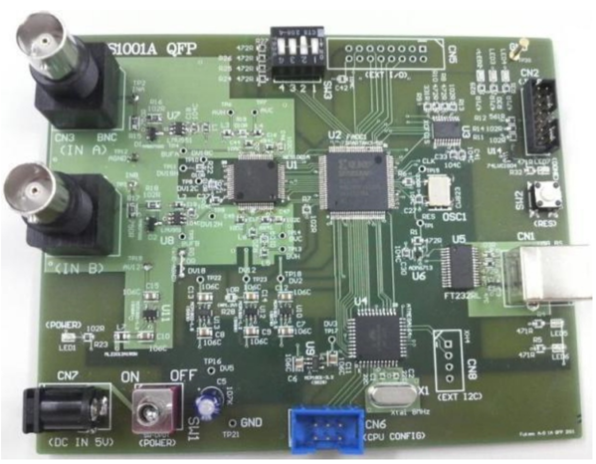

Fig 7 Evaluation board set-up

IX. REFERENCES

[1] Behzad Razavi, Design of Analog CMOS Integrated Circuit.

[2] Samer Medawar1, Peter Händel12, Niclas Björsell2, Magnus Jansson1, ADC Characterization By Dynamic Integral Nonlinearity

[3] Nicholas "Nick" Gray, ABCs of ADCs - Rev 3, June 2006

[4] Sara Qazi, "Study of Time-Interleaved SAR ADC and Implementation of Comparator for High Definition Video ADC in 65nm CMOS Process"

[5] Zwei-Mei Lee, Cheng-Yeh Wang, and Jieh-Tsorng Wu, "A CMOS 15-Bit 125-MS/s Time-Interleaved ADC with Digital Background Calibration"

[6] Tsung-Heng Tsai, Paul J. Hurst, and Stephen H. Lewis, "Time-Interleaved Analog-to-Digital Converters for Digital Communications"

[7] Rob Reeder, Mark Looney, Jim Hand "Pushing the State of the Art with Multichannel A/D Converters"

[8] Jens Sauerbrey,Doris SRoland Theweschmitt-Landsiedel, "A 0.5V, 1μW Successive Approximation ADC"

[9] Jipeng Li,"A 1.8-V 67-mW 10-bit 100-MS/s Pipelined ADC Using Time-Shifted CDS Technique"

[10] Christian Vogel and Gernot Kubin, "analysis and compensation of nonlinearity mismatches in time-interleaved adc arrays"

[11] James Catt, "Generating Precision Clocks for Time-Interleaved ADCs"

[12] Simon M. Louwsma, Ed J.M. van Tuijl, Maarten Vertregt* and Bram Nauta, "A 1.35 GS/s, 10b, 175 mW Time-Interleaved AD Converter in 0.13 μm CMOS"

QuEST

BORN TO ENGINEER

www.quest-global.com